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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,708	12/24/2003	Masayuki Kanazawa	500.43357X00	8324

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EXAMINER	
MOE, AUNG SOE	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,708	KANAZAWA ET AL.	
	Examiner	Art Unit	
	Aung S. Moe	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3,8-10 and 15-17 is/are rejected.

7)☒ Claim(s) 4-7,11-14 and 18-21 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 December 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date see attached.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-2, 8-9 and 15-16 are rejected under 35 U.S.C. 102(a) as being anticipated by Hamazaki Toshinori (Translation of JP 2001-057578).

Regarding claim 1, Toshinori '578 discloses a negative feedback amplifier for a transmitter, comprising:

a vector corrector (i.e., noted the correction circuit 12, 7 and 28 as shown in Figs. 12-13; also see paragraphs 0026, 0042 and 0045) for correcting at least one of a phase and an amplitude of an in-phase component (I) and a quadrature component (Q) of an input base-band signal containing data to be transmitted and outputting said corrected one (i.e., noted from Figs. 2 and 12-13, the correction circuits 12/7/28 contain the memory table 22 to be used for correcting one of the phase and amplitude of the I and Q signals; see paragraphs 0042 and 0048-0049);

adder (i.e., noted the adders 1 & 2 and 3 & 4 as shown in Figs. 12-13) for adding a feedback signal of said in-phase component (I4) to said in-phase component of an output from said vector corrector (i.e., noted the I2 as shown in Fig. 13) and a feedback signal of said quadrature component (Q4) to said quadrature component of said output from said vector corrector (i.e., noted the Q2 as shown in Fig. 13), respectively;

a modulator for orthogonally modulating said in-phase components and said quadrature components of outputs of said adder (i.e., noted the Modulator 7 as shown in Figs. 12-14); a power amplifier (i.e., noted the Amplifier 8 as shown in Figs. 12-14; also see paragraphs 0007) for amplifying an output of said modulator (7);

a demodulator (i.e., noted the Demodulator 9 as shown in Figs. 12-14) for orthogonally demodulating a part of an output of said power amplifier (8) and outputting said feedback signals of said in-phase component and said quadrature component (I4 and Q4); and

said vector corrector serving to perform a correcting operation of canceling an error of at least one of the phase and the amplitude of said in-phase component and said quadrature component occurring in said demodulator (i.e., as shown in Figs. 12-14, with the use of correction circuit 12, 7 and 28, the amplitude and angle error of the demodulator is corrected by subtracting the local inphase/rectangular recovery signals; see paragraphs 0042, 0044+ and 0055-0056).

Regarding claim 2, Toshinori '578 discloses a negative feedback amplifier as claimed in claim 1, further comprising a memory (i.e., see Fig. 2, the memory table 22) for storing a value indicating an error of at least one of the phase and the amplitude to be used for said correcting operation (i.e., paragraph 0026+).

Regarding claim 8, Toshinori '578 discloses a transmitter comprising:

a base-band signal generating unit for generating an in-phase component and a quadrature component of a base-band signal containing data to be transmitted (i.e., noted the I1 and Q1 signals inputted to the circuits 7, 12 and 28); and

a transmitting unit (noted the transmitting unit as shown in Figs. 12-14) for modulating said data and thereby generating a transmission signal, based on the in-phase component and the quadrature component of said base-band signal sent from said base-band signal generating unit (i.e., see paragraphs 0019+), and said transmitting unit including;

a vector corrector (i.e., noted the correction circuit 12, 7 and 28 as shown in Figs. 12-13; also see paragraphs 0026, 0042 and 0045) for correcting at least one of a phase and an amplitude of the in-phase component and the quadrature component of said base-band signal sent from said base-band signal generating unit (i.e., noted from Figs. 2 and 12-13, the correction circuits 12/7/28 contain the memory table 22 to be used for correcting one of the phase and amplitude of the I and Q signals; see paragraphs 0042 and 0048-0049),

adder (i.e., noted the adders 1 & 2 and 3 & 4 as shown in Figs. 12-13) for adding the in-phase component and the quadrature component of the output of said vector corrector (i.e., noted the I2 as shown in Fig. 13) to feedback signals of said in-phase component and said quadrature component, respectively, a modulator (i.e., noted the modulator 7 as shown in Figs. 12-14) for orthogonally modulating the in-phase components and the quadrature components of outputs of said adder,

a power amplifier for amplifying an output of said modulator (i.e., noted the Amplifier 8 as shown in Figs. 12-14; also see paragraphs 0007),

a demodulator (i.e., noted the Demodulator 9 as shown in Figs. 12-14) for orthogonally demodulating a part of an output of said power amplifier (8) and outputting said feedback signal of the in-phase component and the quadrature component, and

said vector corrector serving to perform a correcting operation of canceling an error of at least one of the phase and the amplitude of the in-phase component and the quadrature component occurring in said demodulator (i.e., as shown in Figs. 12-14, with the use of correction circuit 12, 7 and 28, the amplitude and angle error of the demodulator is corrected by subtracting the local inphase/rectangular recovery signals; see paragraphs 0042, 0044+ and 0055-0056).

Regarding claim 9, Toshinori '578 discloses a transmitter as claimed in claim 8, wherein said negative feedback amplifier further comprises a memory (i.e., see Fig. 2, the memory table 22) for storing a value indicating an error of at least one of the phase and the amplitude to be used for said correcting operation (i.e., paragraph 0026+).

Regarding claim 15, Toshinori '578 discloses a method of correcting errors of a phase and an amplitude (i.e., the amplitude/angle error) of a negative feedback amplifier included in a transmitter, comprising the steps of:

vector-correcting at least one of a phase and an amplitude of an in-phase component and a quadrature component of an input base-band signal containing data to be transmitted (i.e., noted from Figs. 2 and 12-13, the correction circuits 12/7/28 contain the memory table 22 to be used for correcting one of the phase and amplitude of the I and Q signals; see paragraphs 0042 and 0048-0049);

adding (i.e., noted the adders 1 & 2 and 3 & 4 as shown in Figs. 12-13) feedback signals of the in-phase component and the quadrature component to the corrected in-phase component and quadrature component, respectively;

orthogonally modulating (i.e., noted the Modulator 7 as shown in Figs. 12-14) said in-phase component and said quadrature component to which said feedback signals are added; amplifying said orthogonally modulated signals (i.e., noted the Amplifier 8 as shown in Figs. 12-14; also see paragraphs 0007); orthogonally demodulating (i.e., noted the Demodulator 9 as shown in Figs. 12-14) a part of said each amplified signal and then outputting said feedback signals of the in-phase component and the quadrature component;

in said correcting step, performing a correcting operation of canceling an error of at least one of the phase and amplitude of the in-phase component and the quadrature component occurring in said demodulator (i.e., as shown in Figs. 12-14, with the use of correction circuit 12, 7 and 28, the amplitude and angle error of the demodulator is corrected by subtracting the local inphase/rectangular recovery signals; see paragraphs 0042, 0044+ and 0055-0056).

Regarding claim 16, Toshinori '578 discloses method as claimed in claim 15, further comprising the step of storing in a memory (i.e., see Fig. 2, the memory table 22) a value indicating an error of at least one of the phase and the amplitude to be used for said correcting operation, and wherein said correcting operation of canceling said error is executed based on the value indicating the error stored in said memory (i.e., paragraph 0026+).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 3, 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshinori '578 in view of Huang et al. (U.S. 6,885,241).

Regarding claims 3 and 10, it is noted that Toshinori '578 does not explicitly show the use of an external device to provide error correction value as claimed.

However, the above-mentioned claimed invention is well known in art as evidenced by Huang '241. In particular, Huang '241 teaches an external device (1413; see col. 12, lines 1-12) to provide error correction value to the vector corrector (i.e., noted the vector corrector 1401 receiving the correction data from the external memory 1413).

In view of the above, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Toshinori '578 as taught by Huang '241, since Huang '241 stated in col. 14, lines 60+ that such a modification would allow the

system to switch between the different reference type information stored within the external memory as the modulation scheme.

Regarding claim 17, Toshinori '578 does not show the use of a test device to an input unit and an output unit of said negative feedback amplifier; when a predetermined testing signal is inputted from said test device to the input unit of said negative feedback amplifier, causing said test device to detect an error of at least one of the phase and the amplitude of the in-phase component and the quadrature component occurring in said demodulator from a signal of said output unit; and putting a value indicating said detected error in said memory.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Huang '241. In particular, Huang '241 teaches the use of a test device (i.e., noted the DSP-1411 and the memory 1413 for calibration of the I and Q data; see col. 12, line1-15) to an input unit and an output unit of said negative feedback amplifier (i.e., noted the feedback Amplifier as shown in Fig. 14a); when a predetermined testing signal (i.e., noted the calibration signals provided by the DSP-1411 and memory 1413) is inputted from said test device (i.e., Figs. 14c, the memory 1413) to the input unit of said negative feedback amplifier (i.e., noted the feedback amplifier as shown in Fig. 14C), causing said test device to detect an error of at least one of the phase and the amplitude of the in-phase component and the quadrature component occurring in said demodulator (i.e., noted demodulator 1419) from a signal of said output unit; and putting a value indicating said detected error in said memory (i.e., noted the memory 1420).

In view of the above, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Toshinori '578 as taught by Huang '241, since Huang '241 stated in col. 14, lines 60+ that such a modification would allow the

system to switch between the different reference type information stored within the external memory as the modulation scheme.

Allowable Subject Matter

6. Claims 4-7, 11-14 and 18-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Following references are related to the present claimed invention:

US 6,112,062	US 5,959,499	US 6,993,091	US 6,693,956
US 6,384,677	US 5,802,451	US 5,469,105	US 6,941,118
US 5,404,378	US 6,381,286	US 6,240,144	US 6,985,704

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aung S. Moe whose telephone number is 571-272-7314. The examiner can normally be reached on Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aung S. Moe
Primary Examiner
Art Unit 2685

A. Moe
March 6, 2006